What Is Claimed Is:

1. An instruction pipeline in a microprocessor, comprising:

a plurality of pipeline units, each of the pipeline units processing instructions, at least one of the plurality of pipeline units receiving the instructions from another of the pipeline units, storing the instructions and reissuing at least one of the instructions after a stall occurs in the instruction pipeline.

2. The instruction pipeline of claim 1, wherein the at least one of the plurality of pipeline units reissues the at least one of the instructions in order.

3. The instruction pipeline of claim 1, wherein the at least one of the plurality of pipeline units stores only valid instructions of the instructions.

4. The instruction pipeline of claim 1, wherein the instructions are distributed in multiple threads for the plurality of pipeline units to process.

5. An instruction pipeline in a microprocessor, comprising:

at least one upstream pipeline unit issuing a first series of instructions and a second series of instructions;

at least one downstream pipeline unit allocating the first series of instructions and the second series of instructions; and

an instruction queue, wherein in a first operating mode, the instruction queue passes the first series of instructions from the at least one upstream pipeline unit to the at least one downstream pipeline unit and stores the first series of instructions, and in a second operating mode the instruction queue stores the second series of instructions and issues at least one of the first series of instructions and the second series of instructions to the at least one downstream pipeline unit.

6. The instruction pipeline of claim 5, wherein the instruction queue includes a memory array storing the first series of instructions and the second series of instructions.

7. The instruction pipeline of claim 6, wherein the at least one of the first series of instructions and the second series of instructions are issued from the memory array.

8. The instruction pipeline of claim 5, wherein the first operating mode is a default operating mode of the instruction queue.

9. The instruction pipeline of claim 5, wherein the instruction queue switches from the first operating mode to the second operating mode after receiving a stall signal from the at least one downstream pipeline unit.

10. The instruction pipeline of claim 9, wherein the at least one downstream pipeline unit includes a resource, and wherein the at least one downstream pipeline unit generates the stall signal when the resource is full.

11. The instruction pipeline of claim 5, wherein the at least one upstream pipeline unit includes a trace cache.

12. The instruction pipeline of claim 5, wherein the at least one upstream pipeline unit issues the first series of instructions in a first predetermined order, and the instruction queue in the first operating mode passes and stores the first series of instructions in the first predetermined order.

13. The instruction pipeline of claim 12, wherein the at least one upstream pipeline unit issues the second series of instructions in a second predetermined order, and the instruction queue in the second operating mode stores the second series of instructions in the second predetermined order, and issues the at least one of the first series of instructions in the first predetermined order prior to issuing the second series of instructions in the second predetermined order.

14. The instruction pipeline of claim 6, wherein the at least one upstream pipeline unit includes a counter, the counter being incremented when the at least one upstream pipeline

unit issues each of the first series of instructions and each of the second series of instructions, the counter being decremented when the at least one downstream pipeline unit allocates each of the first series of instructions and each of the second series of instructions, and wherein when the counter is one of greater than and equal to a predetermined value, the at least one upstream pipeline unit delays in issuing a next one of the first series of instructions and the second series of instructions until the counter is less than the predetermined value.

15. The instruction pipeline of claim 14, wherein the predetermined value is equal to a number of memory locations in the memory array.

16. The instruction pipeline of claim 5, wherein the instruction queue includes:

a memory array for storing the first series of instructions and the second series of instructions; and

an output multiplexer for issuing the at least one of the first series of instructions and the second series of instructions in the second operating mode, the at least one of the first series of instructions and the second series of instructions being sent from the memory array to the output multiplexer when the instruction queue receives a stall signal, and wherein the output multiplexer issues the at least one of the first series of instructions and the second series of instructions when the stall signal clears.

17. An instruction pipeline in a microprocessor, comprising:

at least one upstream pipeline unit issuing each of a series of instructions on one of a plurality of instruction threads;

at least one downstream pipeline unit allocating each of the series of instructions on the one of the plurality of instruction threads which the at least one upstream pipeline issued each of the series of instructions; and

an instruction queue, wherein in a first operating mode, the instruction queue passes each of the series of instructions from the at least one upstream pipeline unit to the at least one downstream pipeline unit on the one of the plurality of instruction threads on which each of the series of instructions were issued and storing each of the series of instructions, at least one memory location being dedicated to each of the plurality of instruction threads, and in a

second operating mode the instruction queue issues to the at least one downstream pipeline unit at least one of the series of instructions on the one of the plurality of instruction threads on which the at least one of the series of instructions was issued.

18. The instruction pipeline of claim 17, wherein the instruction queue in the first operating mode alternates passing the series of instructions on the one of the plurality of instruction threads on which each of the series of instructions were issued when a stall signal is not present on any of the plurality of instruction threads, and when the stall signal is present on one of the plurality of instruction threads, the instruction queue issues the series of instructions on an other one of the plurality of instruction threads.

19. The instruction pipeline of claim 17, wherein the at least one upstream pipeline unit determines the one of the plurality of instruction threads on which to issue each of the series of instructions based the availability of resources on each of the plurality of instruction threads.

20. An instruction queue in an instruction pipeline of a microprocessor, comprising:

at least one memory array; and

an output multiplexer for selecting one of a first instruction source and a second instruction source to output instructions, the second instruction source being selected after the instruction queue receives a stall signal, and wherein the second instruction source is the at least one memory array.

21. The instruction queue of claim 20, further comprising a queue control for receiving the stall signal and controlling the selection by the output multiplexer.

22. The instruction queue of claim 20, the memory array including:

a plurality of memory locations for storing the instructions;

a write pointer indicating a current one of the plurality of memory locations for storing a current one of the instructions;

a read pointer indicating one of the plurality of memory locations storing one of the

instructions for outputting; and

a stall pointer indicating one of the plurality of memory locations storing a first one of the instructions not allocated by the instruction pipeline.

23. A method for processing instructions on a plurality of instruction threads in an instruction pipeline of a microprocessor, the method comprising the steps of:

selecting a first one of the plurality of instruction threads on which to issue at least one instruction;

issuing the at least one instruction on the first one of the plurality of instruction threads when a stall signal is not present on the first one of the plurality of instruction threads;

determining if a stall signal is present on a second one of the plurality of instruction threads;

switching to the second one of the plurality of instruction threads if the stall signal is not present on the second one of the plurality of instruction threads; and

issuing at least one instruction on the second one of the plurality of instruction threads.

24. The method of claim 23 further comprising the step of determining if the at least one instruction is available on the first one of the plurality of instruction threads.

25. The method of claim 23 further comprising the steps of:

monitoring the instruction pipeline to determine which one of the plurality of instruction threads has the most available resources; and

issuing at least one instruction on the one of the plurality of instruction threads having the most resources.

26. A method for processing instructions in an instruction pipeline of a microprocessor, the method comprising the steps of:

issuing instructions for processing by the instruction pipeline;

storing the issued instructions;

reissuing at least one of the stored instructions for further processing by the instruction

pipeline after a stall occurs in the instruction pipeline.

27. The method of claim 26, wherein the at least one stored instruction had not been executed by the instruction pipeline prior to being reissued.